AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-36 (cancelled)

37. (new) An integrated semiconductor structure comprising:

a multijunction solar cell structure having at least first and second subcells; and

a bypass device integral to a subcell for passing current when the solar cell is shadowed and having p-type, i-type, and n-type layers.

38. (new) The structure as defined in claim 37, wherein said structure includes a substrate, wherein the subcells are formed on a first portion of the substrate and said bypass device includes a bypass diode formed on a second portion of the substrate.

39. (new) The structure as defined in claim 38, wherein the layers of the subcells are epitaxially grown in a first process and the active layers of said bypass diode are epitaxially grown over the layers of the subcells in a subsequent second process.

40. (new) The structure as defined in claim 39, wherein said expitaxially grown diode is electrically connected across at least said first and second subcells to protect such first and second subcells against reverse biasing.

41. (new) The structure as defined in claim 39, wherein the bypass diode includes a metal/semiconductor contact.

42. (new) The structure as defined in claim 41, wherein the metal/semiconductor contact is TiAu with InGaP.

43. (new) The structure as defined in claim 41, wherein the metal/semiconductor contact forms a Schottky junction.

44. (new) The structure as defined in claim 38, wherein the substrate is Ge.

45. (new) The structure as defined in claim 37, wherein the second solar subcell is fabricated as least in part with InGaP.

46. (new) The structure as defined in claim 37, wherein the first solar subcell is fabricated at least in part with GaAs.

47. (new) A solar cell semiconductor devise comprising:

a semiconductor body having a sequence of layers of semiconductor material including a first region in which the sequence of layers of semiconductor material forms a sequence of cells of a multijunction solar cell; and

a second region laterally spaced apart from said first region and in which the sequence of layers forms a support for an integral bypass diode to protect said cells against reverse biasing at less than breakdown voltage.

48. (new) A device as defined in claim 47, wherein the sequence of layers of one of said cells and the sequence of layers of the bypass diode are epitaxially grown in the same process step.

49. (new) A device as defined in claim 47, wherein the semiconductor body includes a Ge substrate, and at least one of the solar cells is fabricated at least in part with GaAs.

50. (new) A solar cell semiconductor device comprising:

a semiconductor structure having a sequence of layers of semiconductor material including a first region in which the sequence of layers of semiconductor material forms a sequence of cells of a multijunction solar cell; and

a second region separated from said first region by a trough in said sequence of layers and in which the sequence of layers forms a support for an integral bypass diode to protect the multijunction solar cell against reverse biasing by allowing current to pass when the solar cell is shadowed.

51. (new) A device as defined in claim 50, wherein the sequence of layers said one cell and the sequence of layers of the bypass diode are epitaxially grown in a different process step.

52. (new) A device a defined in claim 50, wherein the semiconductor body includes a Ge substrate, and at least one of the cells is fabricated at least in part with GaAs.

53. (new) A device as defined in claim 50, further comprising

a lateral conduction layer lying over said layers of said second region for electrically connecting the multijunction solar cell to said bypass diode.

54. (new) The device as defined in claim 53, wherein said structure includes a substrate, wherein the subcells are formed on a first portion of the substrate and said bypass diode is formed on a second portion of the substrate over said lateral conduction layer.

55. (new) The device as defined in claim 53, wherein the solar cell and lateral conduction layer are epitaxially grown in a first process and the active layers of said bypass diode are epitaxially grown in a subsequent second process.

56. (new) The device as defined in claim 55, wherein said epitaxially grown diode is electrically connected across at least said first and second subcells to protect such first and second subcells against reverse biasing at less than breakdown voltage.

57. (new) The device as defined in claim 50, wherein the bypass diode includes a metal/semiconductor contact.

58. (new) The device as defined in claim 57, wherein the metal/semiconductor contact is TiAu with InGaP.

59. (new) The device as defined in claim 57, wherein the metal/semiconductor contact forms a Schottky junction.

60. (new) The device as defined in claim 50, wherein said bypass diode includes p-type, i-type, and n-type layers.

61. (new) The device as defined in claim 53, wherein the lateral conduction layer is an n-doped GaAs layer for conducting electrical current.

62. (new) The solar device of claim 60, wherein the p-type layer of the bypass diode is a p-doped GaAs layer and the n-type layer of the bypass diode is an n-doped GaAs layer.

63. (new) The solar device of claim 60, wherein the i-type layer of the bypass diode is a lightly doped GaAs layer for reducing defect breakdown.

64. (new) The solar device of claim 60, wherein the i-type layer of the bypass diode is an undoped GaAs layer for reducing defect breakdown.

65. (new) A solar cell semiconductor device comprising:

a substrate;

a first sequence of layers of semiconductor material deposited on said substrate;

including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell; and

a second region including said first sequence of layers, and a second sequence of layers that forms a bypass diode to protect said cell against reverse biasing at less than breakdown voltage; and

a metal layer deposited on a portion of said substrate and over at least a portion of said second region for electrically shorting the first sequence of layers of said second region and to electrically connect to said bypass diode in said second region.

66. (new) A device as defined in claim 65, further comprising a lateral conduction layer wherein said metal layer forms a shunt having a first contact on the solar cell and a second contact on the bypass diode, wherein said first contact is connected to the substrate to make an electrical connection to the solar cell and said second contact is connected to a lateral conduction layer to make an electrical connection to the bypass diode.

67. (new) A device as defined in claim 65, further comprising a trough situated between the solar cell and the bypass diode that provides electrical isolation between the solar cell and the diode.

68. (new) A device as defined in claim 66, further comprising a stop etch layer deposited over the lateral conduction layer.

69. (new) A device as defined in claim 65, wherein said bypass diode includes p-type, i-type, and n-type layers.

70. (new) A device as defined in claim 66, wherein the lateral conduction layer is an n-doped GaAs layer for conducting electrical current.

71. (new) A solar divide of claim 69, wherein the p-type layer of the bypass diode is a p-doped GaAs layer and the n-type layer of the bypass diode is an n-doped GaAs layer.

72. (new) A solar device of claim 69, wherein the i-type layer is a lightly doped GaAs layer for reducing defect breakdown.

73. (new) A solar device of claim 69, wherein the i-type layer is an undoped GaAs layer for reducing defect breakdown.

74. (new) A method of making an integrated semiconductor structure comprising:

forming a multijunction solar cell structure having at least first and second subcells; and

subsequently forming a bypass device having p-type, i-type, and n-type layers integral to the semiconductor structure to allow the current to pass through the bypass device when a solar cell is shadowed.

75. (new) The method as defined in claim 74, wherein said structure includes a substrate, wherein the subcells are formed on a first portion of the substrate and said bypass device is a bypass diode formed on a second portion of the substrate.

76. (new) The method as defined in claim 75, wherein the subcells are epitaxially grown in a first process and the active layers of said bypass diode are epitaxially grown in a subsequent second process.

77. (new) The method as defined in claim 76, further comprising electrically connecting the bypass diode across at least said first and second subcells to protect such first and second subcells against reverse biasing.

78. (new) The structure as defined in claim 75, further comprising forming a metal/semiconductor contact on the bypass diode to form a Schottky junction.

79. (new) A method of making a solar cell semiconductor device comprising:

depositing a sequence of layers of semiconductor material on a substrate including forming a first region in which the sequence of layers of semiconductor material forms a sequence of cells of a multijunction solar cell; and

forming a second region laterally spaced apart from said first region and which the sequence of layers forms a support for an integral bypass diode to allow current to pass when the solar cell is shadowed.

80. (new) A method as defined in claim 79, wherein depositing the sequence of layers of said solar cell and the sequence of layers of the bypass diode are performed by epitaxial growth in the same process step.

81. (new) A method as defined in claim 79, further comprising providing a Ge substrate, and fabricating at least one of the solar cells in the Ge substrate.

82. (new) A method of making a solar cell semiconductor device comprising:

providing a substrate;

depositing a sequence of layers of semiconductor material on said substrate, including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell, and a second region in which the sequence of layers forms a bypass diode; and

depositing a lateral conduction layer over said layers of said first and second region.

83. (new) A method as defined in claim 82, further comprising forming the subcells on a first portion of the substrate and forming said bypass diode on a second portion of the substrate over said lateral conduction layer in said second region.

84. (new) A method as defined in claim 82, further comprising growing the solar call and the lateral conduction layer in a first process and growing the active layers of said bypass diode in a subsequent second process.

85. (new) A method as defined in claim 82, further comprising connecting the bypass diode across at least first and second subcells of said multijunction solar cell to protect said first and second subcells against reverse biasing at less than breakdown voltage.

86. (new) An integrated semiconductor structure comprising:

a multijunction solar cell including first and second solar cells on a first portion of the semiconductor structure;

means integral to a second portion of said semiconductor structure overlying said first portion for passing current when said multijunction solar cell is shaded; and

a metal layer connecting said multijunction solar cell and said means for passing current, wherein one end of said metal layer is coupled to the base of said first solar cell and another end of said metal layer is coupled to one terminal of said means for passing current.

87. (new) The structure as structure as defined in claim 86, wherein said first solar cell is formed on a first portion of the substrate, and said means for passing current is a bypass diode formed on a second portion of the substrate.

88. (new) The structure as defined in claim 87, wherein said first portion and said second portion are separated by a trough, and said metal layer lies over said trough.

89. (new) The structure as defined in claim 86, wherein said first and second solar cells grown in a first process and said bypass diode is formed in a subsequent process.

90. (new) A solar cell semiconductor device comprising:

an integral semiconductor body having a sequence of layers of semiconductor material including a first region in which the sequence of layers of semiconductor material forms a sequence of cells of a multijunction solar cell; and

a second region laterally spaced apart from said first region and in which the sequence of layers corresponding to the sequence of layers forming said cells forms a support structure for a bypass diode to protect said multijunction solar cell against reverse biasing at less than breakdown voltage.

91. (new) A device as defined in claim 90, wherein the sequence of layers of said multijunction solar cell and the sequence of layers of the support structure are formed in the same process step.

92. (new) A device as defined in claim 90, wherein the bypass diode is fabricated at least in part with GaAs.

93. (new) A solar cell semiconductor devise comprising:

a substrate;

a sequence of layers of material deposited on said substrate, including a first region in which the sequence of layers of material forms a plurality of cells of a multijunction solar cell, and a second region which the corresponding sequence of layers forms a support for a bypass diode to protect said cell against reverse biasing; and

a lateral conduction layer deposited over said sequence of layers for making electrical contact to an active region of said bypass diode.

94. (new) A device as defined in claim 93, wherein said lateral conduction layer in the first region is physically separated from the lateral conduction layer in the second region.

95. (new) A device as defined in claim 93, wherein said lateral conduction layer is a highly doped layer.

96. (new) A device as defined in claim 95, wherein said lateral conduction layer is composed of GaAs.

97. (new) A device as defined in claim 93, further comprising an etch stop layer, deposited over said lateral conduction layer.

98. (new) A device as defined in claim 93, wherein said substrate forms an electrical connection path between said multijunction solar cell as said bypass diode.

99. (new) A device as defined in claim 93, further comprising

a metal layer deposited on a portion of said substrate and over at least a portion of said second region and functioning to (i) electrically short layers of said second region, and (ii) connect the substrate to said lateral conduction layer to complete the electrical circuit between the multijunction solar cell and the bypass diode.

100. (new) A solar cell semiconductor device comprising:

a substrate;

a sequence of layers of semiconductor material deposited on said substrate including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell, and a second region in which the corresponding sequence of layers forms a bypass diode to protect said cell against reverse biasing; and

wherein said sequence of layers includes a lateral conduction layer including a first portion disposed in said first region, and a second portion disposed in said second region and physically separated from said first portion.

101. (new) A device as defined in claim 100, wherein said lateral conduction layer is a highly doped layer.

102. (new) A device as defined in claim 100, wherein said lateral conduction layer is composed of GaAs.

103. (new) A device as defined in claim 100, wherein one of the layers of said sequence of layers is a cap layer, and said lateral conduction layer is disposed directly over said cap layer.

104. (new) A device as defined in claim 100, wherein said second portion of said lateral conduction layer makes electrical contact with a layer of said bypass diode.

105. (new) A device as defined in claim 100, wherein said bypass diode comprises an n GaAs layer, and a p GaAs layer disposed over said n GaAs layer.

106. (new) A device as defined in claim 100, further comprising a metal layer deposited on a portion of said substrate and over at least a portion of said second region and functioning to connect the substrate to a portion of said lateral conduction layer for completing the electrical circuit between the multijunction solar cell and the bypass diode.

107. (new) A solar cell semiconductor device comprising:

a substrate;

a sequence of layers of semiconductor material deposited on said substrate, including a first region in which the lower portion of said sequence of layers of semiconductor material forms a multijunction solar cell, and a second region in which the corresponding sequence of layers above said lower portion forms a bypass diode to protect said cell against reverse biasing at less than breakdown voltage; and

a highly conductive lateral conduction layer deposited over the portion of said sequence of layers forming the multijunction solar cell, for making electrical contact with one layer of said bypass diode and forming a contact region to allow said bypass diode to be electrically connected to said multijunction solar cell.

108. (new) A device as defined in claim 107, further comprising a metal layer deposited on a portion of said substrate and over at least a portion of said second region and functioning to connect the substrate to a portion of said lateral conduction layer for completing the electrical circuit between the multijunction solar cell and the bypass diode.

109. (new) A device as defined in claim 107, wherein said lateral conduction layer includes a first portion disposed in said first region, and a second portion disposed in said second region and separated from the first portion.

110. (new) A device as defined in claim 107, wherein said lateral conduction layer is composed of GaAs.

111. (new) A device as defined in claim 109, wherein said second portion of said lateral conduction layer makes electrical contact with a first active layer of said bypass diode.